REMARKS

This responds to the Office Action mailed on August 4, 2008. Claims 1 and 8 are amended, and no claims are canceled, or added; as a result, claims 1, 3, and 7-14 are now pending in this application.

35 USC §103 Rejection of the Claims

Claims 1 and 8 were rejected under 35 USC § 103(a) as being unpatentable over DeWitt (U.S. Patent No. 3,727,147) and further in view of Carroll et al. (U.S. Patent No. 3,972,020). Claims 1 and 8 have been amended to further clarify the claimed invention. Individual limitations in claims 1 and 8 are now discussed.

Independent Claim 1

Claim 1 has been amended to clearly recite the structure that forms the parallel differential input stages of the common mode rejection amplifier. Applicants respectfully submit that the cited references, taken alone or in combination, fail to disclose, teach or suggest the subject matter of claim 1 as amended. Individual limitations recited in claim 1 are now discussed.

input amplifier having first and second differential outputs

Claim 1 has been amended to recite an input amplifier rather an "input stage" to differentiate this element from the input stages of the common mode rejection amplifier. The input amplifier has first and second differential outputs. This corresponds to input stage 210 (Figure 2), a more detailed embodiment of which is shown at 310 (Figure 3), readily recognizable by one of skill in the art as an amplifier. First and second differential outputs are shown at 206 and 208. Applicants respectfully submit that the cited references, taken alone or in combination, fail to disclose, teach, or suggest an "input amplifier having first and second differential outputs" as recited in claim 1.

a common mode rejection amplifier including first and second input transistors to form a first differential input stage, and third and fourth input transistors to form a second differential input stage, the first and second differential input stages coupled in parallel

This claim limitation corresponds to the two parallel-coupled differential input stages shown in Figure 3 of the application as filed. The first differential input stage is formed by first transistor 326 and second transistor 324, and the second differential input stage is formed by third transistor 322 and fourth transistor 328. Applicants respectfully submit that the cited references fail to disclose two parallel-coupled differential input stages formed from differential transistor pairs as recited in claim 1.

wherein the first and third low pass filters are coupled to provide signals to the first and second input transistors, respectively, of the first differential input stage, and the second and fourth low pass filters are coupled to provide signals to the third and fourth input transistors, respectively, of the second differential input stage

This claim limitation provides an explicit recitation of the connections between the four low pass filters and the two parallel differential input stages of the common mode rejection amplifier. The connections recited in this claim limitation are illustrated as connections between low pass filters 110, 120, 130, and 140, and transistors 322, 324, 326, and 328 in Figure 3. Applicants respectfully submit that the cited references, taken alone or in combination, fail to disclose, teach, or suggest this claim limitation.

Independent Claim 8

The subject matter of claim 8 corresponds to band pass filter 200 (Figure 2) without the input stage 210. The first and second differential input nodes correspond to node 206 and 208. The four low pass filters are shown at 110, 120, 130, and 140. The differential amplifier with two parallel input stages is shown at 220, with a more detailed embodiment shown at 320 in Figure 3. Claim 8 has been amended similar to claim 1 to clearly recite the structure that forms the parallel differential input stages of the differential amplifier. Claim 8 now clearly recites the interconnection between the four low pass filters and the transistors of the two parallel coupled differential input stages of the differential amplifier as shown in Figure 3. Applicants

respectfully submit that the cited references, taken alone or in combination, fail to disclose, teach or suggest the subject matter of claim 8 as amended.

Claims 3, 7, 9 and 14 were rejected under 35 USC § 103(a) as being unpatentable over DeWitt (U.S. Patent No. 3,727,147) and further in view of Carroll et al. (U.S. Patent No. 3,972,020) and Isberg et al. (U.S. Patent No. 6,029,052). Claims 10-13 were rejected under 35 USC § 103(a) as being unpatentable over DeWitt (U.S. Patent No. 3,727,147) and further in view of Isberg et al. (U.S. Patent No. 6,029,052) and Fanous et al. (U.S. Publication No. 2003/02060663A1).

These rejections rely on the rejections of independent claims 1 and 8 under 35 USC *§* 103(a). Applicants respectfully submit that the rejections of claims 1 and 8 have been overcome. Accordingly, applicants believe that the claim rejections of the dependent claims under 35 USC *§* 103(a) has also been overcome.

Conclusion

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (952-473-8800) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-4238.

Respectfully submitted,

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